



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION OF: ANDREAS HERKERSDORF, ET AL  
DATED: September 12, 2002  
SERIAL NO. 10/658,311  
DOCKET NO. CH919990056US1

FOR: METHOD FOR PROCESSING A DATA PACKET

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents  
Alexandria, VA 22313

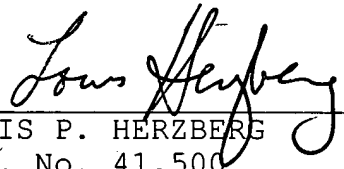
Sir:

Attached are a PTO-1449 form and copies of listed references for  
your consideration in the prosecution of the application above.

A fee required under 37 C.F.R. 1.17(p) is authorized to be  
charged to Deposit Account Number 09-0468.

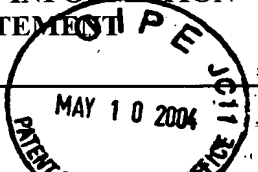
Respectfully submitted,

By:

  
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05/11/2004 SSESHE1 00000126 090468 10658311  
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<b>FORM PTO-1449 (Modified)</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>	<b>ATTY. DOCKET NO.</b> CH9/2002/0009US1	<b>SERIAL NO.</b> 10/658,311
	<b>APPLICANT: ANDREAS HERKERSDORF, ET AL</b>	
	<b>FILING DATE:</b> Herewith	<b>GROUP:</b>

**REFERENCE DESIGNATION**
**U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA	US2002/0091856	7/11/02	D.A. Brown	709/238	G06F15/173	10/31/01

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AB	EP 1,011 231	06/21/00	EP	H04L /12/56	H04L29/06		
	AC	EP 1,122,927	08/08/01	EP	H04L/29/06	H04L12/56		

**OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)**

	AD	IP Caching For Terabit Speed Routers, B. Talbot, T. Sherwood, B. Lin, GlobeCom'99, 1999 IEEE, pp. 1565-1569						
	AE	Performance Evaluation Of Hierarchical Caching In High-Speed Routers, E. Besson, P. Brown, Globe Com'98, 1998 IEEE, pp. 2640-2645						
	AF	Improving Gateway Performance With A Routing-Table Cache, David C. Feldmeier, InfoCom'88, 1988 IEEE, pp. 298-307						
	AG	High-Performance IP Routing Table Lookup Using CPU Caching, Tzi-cker Chiueh, Prashant Pradhan, InfoCom, 1999, IEEE , pp. 1421-1428						
	AH	Cache Memory Design For Internet Processors, Tzi-cker Chiueh, Prashant Pradhan, InfoCom 2000 IEEE, pp. 2-7						
	AI	Router Plugins: A Software Architecture for Next-Generation Routers, Dan DeCasper, Zubin Dittia, Guru Prulkar and Bernhard Plattner, IEEE/ACM Transactions On Networking, Vol. 8, No. 1, February 2000, pp. 135-140						
	AJ	A Novel Cache Architecture to Support Layer-Four Packet Classification at Memory Access Speeds, Jun Xu, Mukesh Singhal, Joanne Degroat, IEEE, InfoCom, 2000, pp. 1445-1454						

**EXAMINER**
**DATE CONSIDERED**

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of: Andreas Herkersdorf , et al.

Serial No.: 10/658,311

Filed: September 12, 2002

Group Art:

For: **METHOD FOR PROCESSING A DATA PACKET**

Assistant Commissioner for Patents  
Alexandria, VA 22313-1450

**CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)**

I hereby certify that the attached correspondence comprising:

1. Information Disclosure Statement
2. Postcard

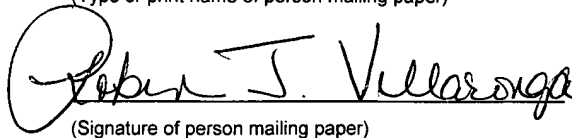
is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

*Assistant Commissioner for Patents*  
Alexandria, VA 22313-1450

on May 5, 2004.

ROBIN J. VILLARONGA

(Type or print name of person mailing paper)



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Docket No.: CH919990056US1